CLAIMS

1. (Previously Amended) A semiconductor device, comprising:

a substrate having circuitry formed therein;

a passivation layer formed overlying at least a portion of the substrate;

a fuse, which may be selectively open-circuited, formed overlying the passivation layer; and

a packaging material formed in contact with the fuse, wherein the packaging material is selected from the group consisting of a mold compound and an underfill; and, wherein the circuitry comprises a first circuit and a second circuit, the semiconductor device further comprising:

a first interconnect for electrically connecting the first circuit to a first portion of the fuse; and

a second interconnect for electrically connecting the second circuit to a second portion of the fuse,

wherein the first circuit and the second circuit are no longer electrically connected if the fuse is open-circuited .

2. (Original) A semiconductor device as in claim 1, wherein a recessed area is formed in the passivation layer and wherein at least a portion of the fuse is formed in the recessed area.

3. (Original) A semiconductor device as in claim 1, wherein the fuse comprises a metal.

4. (Original) A semiconductor device as in claim 3, wherein the fuse comprises aluminum.

5. (Original) A semiconductor device as in claim 1, wherein the fuse comprises a metal nitride.

6. (Original) A semiconductor device as in claim 1, wherein the fuse comprises a metal and a metal nitride.

7. (Original) A semiconductor device as in claim 1, wherein the fuse comprises a metal having a thickness less than approximately 1 micron.

8. (Previously Canceled)

9. (Original) A semiconductor device as in claim 1, wherein the fuse is electrically connected to only the circuitry, and is not electrically connected to anything external to the circuitry.

10. (Previously Canceled)

11. (Currently Amended) A semiconductor device, comprising:

a substrate having a first circuit formed therein, a second circuit formed therein, and a fuse, wherein:

the first circuit has a first contact area,

the second circuit has a second contact area; and

the fuse, which may be selectively open-circuited, is formed overlying the passivation layer, the fuse having a third contact area which is electrically coupled to the first contact area of the first circuit, and the fuse having a fourth contact area which is electrically coupled to the second contact area of the second circuit, wherein the first contact area of the first circuit and the second contact area of the second circuit are no longer electrically connected if the fuse is open-circuited;

a first interconnect for electrically connecting the first contact area to a first portion of the fuse; and

a second interconnect for electrically connecting the second contact area to a second portion of the fuse,

a passivation layer formed overlying at least a portion of the substrate, wherein the fuse is formed overlying the passivation layer; and

a packaging material formed in contact with ~~over~~ the fuse, wherein the packaging material is selected from the group consisting of a mold compound and an underfill.

12. (Original) A semiconductor device as in claim 11, wherein a recessed area is formed in the passivation layer and wherein at least a portion of the fuse is formed in the recessed area.

13. (Original) A semiconductor device as in claim 11, wherein the fuse comprises a metal.

14. (Original) A semiconductor device as in claim 13, wherein the fuse comprises aluminum.

15. (Original) A semiconductor device as in claim 11, wherein the fuse comprises a metal nitride.

16. (Original) A semiconductor device as in claim 11, wherein the fuse comprises a metal and a metal nitride.

17. (Original) A semiconductor device as in claim 11, wherein the first contact area of the first circuit and the second contact area of the second circuit are electrically connected only by way of the fuse.

18. (Previously Amended) A method for forming a semiconductor device having a fuse, comprising:

providing a substrate;

forming a passivation layer overlying at least a portion of the substrate;

forming the fuse overlying the passivation layer;

forming circuitry within the substrate, wherein forming the circuitry comprises

forming a first circuit and forming a second circuit;

forming a first interconnect for electrically connecting the first circuit to a first portion of the fuse; and

forming a second interconnect for electrically connecting the second circuit to a second portion of the fuse, wherein the first circuit and the second circuit are no longer electrically connected if the fuse is open-circuited; and

forming a packaging material in contact with the fuse, wherein the packaging material is selected from the group consisting of a mold compound and an underfill.

19. (Previously Canceled)

20. (Previously Amended) A method of claim 18, further comprising:

blowing the fuse before forming a packaging material.

21. (Previously Amended) A semiconductor device as in claim 11, wherein the packaging material is formed on the fuse.

22. (Previously Canceled)